PATENT ABSTRACTS OF JAPAN

(11)Publication number : **07-240458**

(43)Date of publication of application : **12.09.1995**

(51)Int.Cl. H01L 21/68
H01L 21/3065
// B23Q 17/00

(21)Application number : **06-031612**

(22)Date of filing : **01.03.1994**

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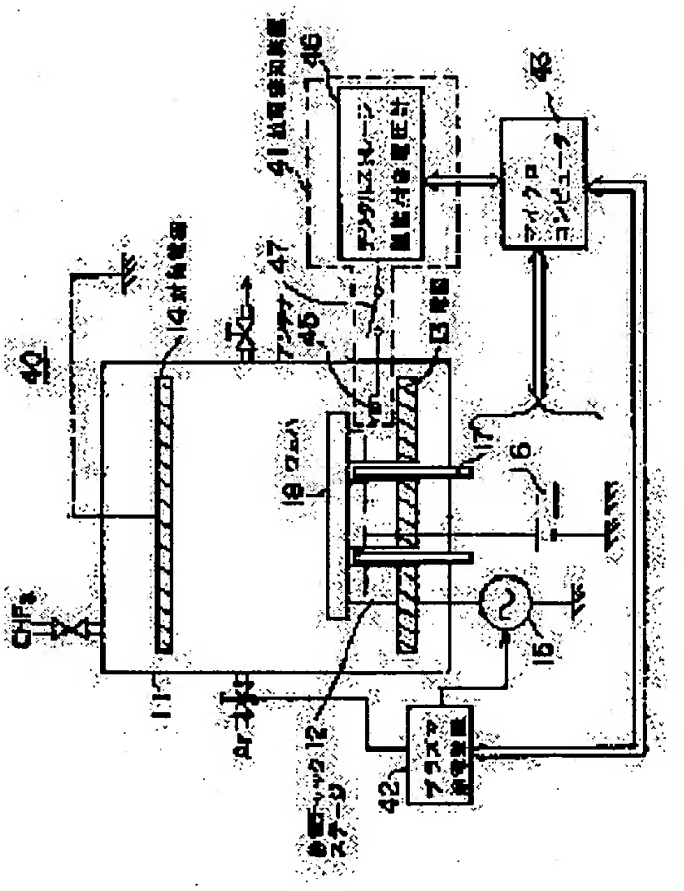
(54) METHOD AND EQUIPMENT FOR PROCESSING SEMICONDUCTOR SUBSTRATE

(57)Abstract:

PURPOSE: To provide a method and equipment for processing a wafer in which the yield is prevented from decreasing due to discharge which may take place at the time of releasing the wafer.

CONSTITUTION: An electrostatic chuck stage 12 for securing a wafer 18 and electrodes 13, 14 for generating plasma are disposed in a vacuum chamber 11. The processing equipment 40 is provided with a unit 41 for sensing discharge which may take place between the wafer 18 and the stage 12 when the wafer 18 is levitated from the stage 12 and released. The discharge sensing unit 41 comprises an antenna 45 and a voltmeter 46. Only when the unit 41 detects discharge, charges are removed from a next wafer 18 subjected to plasma etching.



LEGAL STATUS

[Date of request for examination]	26.02.2001
[Date of sending the examiner's decision of rejection]	30.09.2003
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]	
[Date of final disposal for application]	
[Patent number]	3664745
[Date of registration]	08.04.2005

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CLAIMS

[Claim(s)]
[Claim 1] The semi-conductor substrate processor characterized by considering as the configuration which has a discharge sensing means to sense the discharge which may be generated when making the above-mentioned semi-conductor substrate which finished plasma treatment secede from the above-mentioned stage in the semi-conductor substrate processor which processes to the semi-conductor substrate fixed on the stage.
[Claim 2] The semi-conductor substrate processor according to claim 1 characterized by having an electrification removal means for disappearing electrification of a semi-conductor substrate according to it when said discharge sensing means detects discharge.
[Claim 3] It is the art of the semi-conductor substrate characterized by discharging electrification of a substrate when it has the process which performs plasma treatment to the semi-conductor substrate fixed on the stage, and the process which makes the semi-conductor substrate which finished this plasma treatment secede from this stage, discharge between this substrate and a stage is detected after this process from which it is made to secede and discharge is detected.

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CLAIMS

[Claim(s)]
[Claim 1] The semi-conductor substrate processor characterized by considering as the configuration which has a discharge sensing means to sense the discharge which may be generated when making the above-mentioned semi-conductor substrate which finished plasma treatment secede from the above-mentioned stage in the semi-conductor substrate processor which processes to the semi-conductor substrate fixed on the stage.
[Claim 2] The semi-conductor substrate processor according to claim 1 characterized by having an electrification removal means for disappearing electrification of a semi-conductor substrate according to it when said discharge sensing means detects discharge.
[Claim 3] It is the art of the semi-conductor substrate characterized by discharging electrification of a substrate when it has the process which performs plasma treatment to the semi-conductor substrate fixed on the stage, and the process which makes the semi-conductor substrate which finished this plasma treatment secede from this stage, discharge between this substrate and a stage is detected after this process from which it is made to secede and discharge is detected.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to a semi-conductor substrate processor and an approach, and relates to the equipment and the approach of carrying out plasma treatment to the wafer on an electrostatic chuck stage especially.
[0002] As for a semi-conductor substrate processor, it is desirable that it is the configuration that it can process rationally.
[0003]
[Description of the Prior Art] Drawing 8 shows the conventional plasma etching system 10.
[0004] 11 is a vacuum chamber.
[0005] In the vacuum chamber 11, the electrostatic chuck stage 12, the electrode 13, and the counterelectrode 14 are formed.
[0006] As for RF power source and 16, 15 is [the power source for electrostatic chuck stages and 17] the pins for wafer balking.
[0007] Equipment 10 fixes a wafer 18 according to Coulomb force on the electrostatic chuck stage 12, and is CHF3 in the vacuum chamber 11. Gas is introduced, the plasma is generated between an electrode 13 and 14, plasma etching is performed to the top face of a wafer 18, and after plasma-etching termination, a pin 17 is made to upper-**, a wafer 18 is thrust up, and the actuation from which it is made to float and secede from the electrostatic chuck stage 12 is repeated, and is performed.
[0008]
[Problem(s) to be Solved by the Invention] A wafer 18 tends to be charged by the plasma by the electrostatic chuck stage 12 generated [which generated and electrostatic-fixed]. When floating a wafer 18 depending on [stage / 12 / electrostatic / chuck] the situation of electrification and making it secede from it, as shown in drawing 9 , spark discharge 20 may occur between a wafer 18 and the electrostatic chuck stage 12.
[0009] When discharge occurred, the part where discharge broke out depending on the situation of discharge is damaged and a semiconductor chip is cut down from a wafer, the semiconductor device with which the semiconductor chip including the damaged part was incorporated will become a defective.
[0010] With conventional equipment 10, even if discharge broke out, this was not found, but plasma etching was continued to the wafer one after another, the semiconductor devices of a defective increased in number as a result, and the yield of a semiconductor device was falling.
[0011] In addition, whenever it processes one wafer, supposing it discharges electricity by building the electric discharge plasma, the above-mentioned discharge does not break out but generating of the defect resulting from discharge can be prevented.
[0012] However, in order to build the electric discharge plasma, it is CHF3 in the vacuum chamber 11. The activity which extracts gas and introduces Ar gas will be needed, and an electric discharge activity will take about 2 minutes. works -- setting -- many -- when processing several wafers one after another, the manhour which electric discharge takes will become what cannot be disregarded, and the productivity of a semiconductor device will become low.
[0013] Then, this invention aims at offering the semi-conductor substrate processor and approach which solved the above-mentioned technical problem.
[0014]
[Means for Solving the Problem] As shown in drawing 1 , the semi-conductor substrate processor 30 of this invention processes to the semi-conductor substrate 32 fixed on the stage 31.

[0015] Equipment 30 has the discharge detection means 33.
[0016] The discharge sensing means 33 senses the discharge which may be generated when floating and making it secede from the semi-conductor substrate 32 which finished processing from a stage 31.
[0017]
[Function] The configuration which established the discharge sensing means 33 acts so that it may make it know that the semi-conductor substrate 32 needs to discharge electricity.
[0018]
[Example] Drawing 2 shows the plasma etching system 40 which becomes one example of this invention.
[0019] The same sign is given to the component shown in drawing 8 , and a corresponding part among this drawing, and the explanation is omitted.
[0020] Equipment 40 is added to the equipment 10 of drawing 8 , and has discharge sensing equipment 41, the plasma electric discharger 42, and a microcomputer 43.
[0021] Discharge sensing equipment 41 is arranged near the electrostatic chuck stage 12 in in the vacuum chamber 11, it connects with the antenna 45 which detects the potential distribution between the wafer 18-electrostatic chuck stages 12, and an antenna 45, and it is arranged out of the vacuum chamber 11, and has the voltmeter 46 with a digital storage function which memorizes a voltage waveform.
[0022] The normally open switch 47 is formed in the middle of wiring currently pulled out out of the vacuum chamber 11 from the antenna 45.
[0023] Equipment 40 is controlled by the microcomputer 43, and as shown in drawing 3 , it operates.
[0024] Fundamentally, equipment 40 operates like the equipment 10 of aforementioned drawing 8 .
1 Perform plasma etching to the wafer 18 which was carried in the vacuum chamber 11 and fixed on the electrostatic chuck stage 12 (ST1).
[0025] After plasma etching is completed, the switch 47 which is made to generate the plasma and which carried out relation top Kaisei is closed, and discharge sensing equipment 41 is made into the condition which can be discharge sensed.
2 Thrust up a wafer 18, float and make it to make a power source 16 off, to make a pin 17 upper-**, and secede from the wafer 18 by which plasma etching was carried out from the electrostatic chuck stage 12 (ST2).
3 Judge whether discharge broke out between the wafer 18 and the electrostatic chuck stage 12 at the time of balking based on the information on the voltmeter 46 at the time of this balking (ST3).
4 When the decision result of ST3 is "NO", perform plasma etching to the wafer which returned to ST1 and was carried into the degree.
5 When the decision result of ST3 is "YES", set n with 0 (ST4).
6 Subsequently, add 1 and consider as n=n +1 (ST5).
7 Subsequently, perform plasma etching to the wafer carried into the degree (ST6).
8 After plasma etching is completed, operate the plasma electric discharger 42 (ST7).
[0026] Namely, CHF3 in the vacuum chamber 11 Gas is extracted, Ar gas introduces instead, the RF power source 15 is switched on in this condition, and the plasma is generated among power sources 13 and 14. Thereby, electrification of a wafer is removed and discharged.
9 Subsequently, make a power source 16 off, thrust up a wafer 18 by the pin 17, float and make it secede from a wafer from the electrostatic chuck stage 12 (ST8).
10 Subsequently, compare n with N (ST9).
[0027] N is set to 5. That is, it is N= 5.
[0028] When an artificer experimented, once discharge occurred, it was referred to as N= 5 because generating about about five wafers processed continuously succeeding the time of seceding from a stage, and discharge being subsided and stopping occurring after that understood.
[0029] ST1 will be performed, if ST5 is performed and a decision result serves as "NO", when the decision result of ST9 is "YES."
[0030] Therefore, once discharge is sensed, a loop formation with electric discharge processing (ST5 ->ST6 ->ST7 ->ST8 ->ST9 ->ST5) is entered, and after ending plasma-etching processing and performing electric discharge processing about five wafers following this, it will break away from the electrostatic chuck stage 12, and discharge will not break out at the time of balking.
[0031] After performing plasma-etching processing, it secedes from the wafer of six-sheet memory from the electrostatic chuck stage 12, without performing electric discharge processing. Since, as for discharge, it has already stopped being able to occur easily also at this time, discharge does not break out.

[0032] That is, equipment 40 operates, as shown in drawing 4 to the wafer by which sequential carrying in is carried out.
[0033] In A, plasma etching and B show balking [stage / of a wafer], and C shows electric discharge.
[0034] When discharge resumes while processing the wafer after after [discharge generating] six-sheet memory, electric discharge processing is performed to the following five sheets.
[0035] That is, whenever equipment 40 repeats actuation of plasma-etching -> balking, without usually performing electric discharge processing, and performs it and discharge occurs, it continues operating, operating plasma-etching -> electric discharge -> balking about the following five wafers.
[0036] Therefore, according to above equipment 40, it has the following effectiveness.
[0037] I. The count of the discharge generated at the time of balking of a wafer can be held down to about [in the case of conventional equipment] 1/5, it is [in the case of conventional equipment] few to about 1/5, the number of the defects who therefore originate in discharge can be carried out, and the yield of a semiconductor device may be improved.
[0038] Since II. electric discharge is a configuration performed only when required, it may improve the effectiveness of processing of a wafer compared with the case where electricity is discharged about all wafers.
[0039] For example, when 100 wafers were processed, and the process of plasma-etching-electric discharge-balking was taken about all wafers, to requiring for 3 hours and 30 minutes, according to the above-mentioned equipment 40, it completed in 2 hours and 40 minutes, and time amount compaction for 50 minutes was achieved.
[0040] In addition, since the voltmeter 46 in drawing 2 is what has the digital storage function, it can observe the situation of discharge by the eye.
[0041] When discharge is spark discharge, the sharp voltage waveform shown in drawing 5 (A) with a sign 50 is observed.
[0042] In the case of glow discharge, the voltage waveform of the abbreviation trapezoidal shape shown in drawing 5 (B) with a sign 51 is observed.
The modification of [Modification(s)], next discharge sensing equipment is explained.
[0043] The discharge sensing equipment 60 of drawing 6 is a configuration which consists of an optical fiber 61 which is arranged so that tip 61a may be located near the electrostatic chuck stage 12, and is pulled out out of the vacuum chamber 11, and optical intensimeter 62 connected to the optical fiber 61.
[0044] According to this configuration, the switch 47 in drawing 2 is unnecessary.
[0045] The discharge sensing equipment 70 of drawing 7 is the configuration of having used the arm 71 which conveys a wafer as an antenna 45 in drawing 2 .
[0046] The voltmeter 46 is electrically connected with the arm 71.
[0047] According to this configuration, the antenna 45 of dedication in drawing 2 is unnecessary, and its switch 47 is also unnecessary. Moreover, the discharge generated in the top-face side of a wafer can also be sensed.
[0048] In addition, this invention can be applied also to the configuration which also equipped with stages other than an electrostatic chuck stage the equipment which performs processing of those other than plasma etching again.
[0049] Moreover, in the equipment equipped with the electrostatic chuck stage 12 like the above-mentioned example, it can use as information when judging whether abnormalities generated the frequency of generating of the above-mentioned discharge etc. on the electrostatic chuck stage 12.
[0050] Moreover, when generating of discharge has been sensed, it can be made to stop for electric discharge of equipment 40.
[0051] Moreover, electric discharge of a wafer can also be performed by impressing the electrical potential difference of reversed polarity with the time of all the electrodes of the electrostatic chuck stage 12, and wafer immobilization.
[0052] Moreover, when discharge is glow discharge, the part in which the circuit on a wafer is formed is not damaged.
[0053] Then, when it is detected that discharge broke out, a pressure can be raised somewhat, and the inside of the vacuum chamber 11 can also be constituted so that it may control to consider as the pressure (about 0.2 Torr(s)) to which glow discharge may happen.
[0054]
[Effect of the Invention] As explained above, according to this invention, it has the following effectiveness.
[0055] ** To not knowing, it keeps on discharge having taken place for processing of a semi-conductor substrate, many defects are generated, it can prevent un-arranging [of reducing the yield of a semiconductor device], and the yield of a semiconductor device may be improved compared with the former.
[0056] ** Since electric discharge can be performed only when electric discharge is needed, compared with the case where electricity is discharged at every processing, the manhour which electric discharge takes can be shortened and

the productivity of a semiconductor device may be improved.

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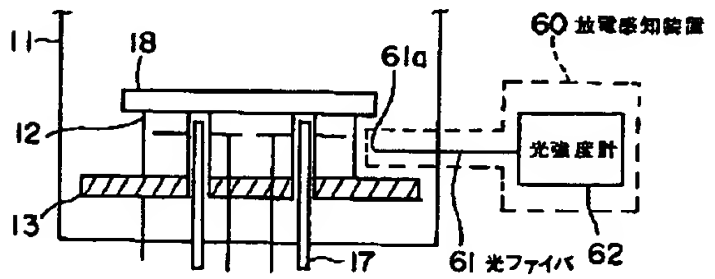
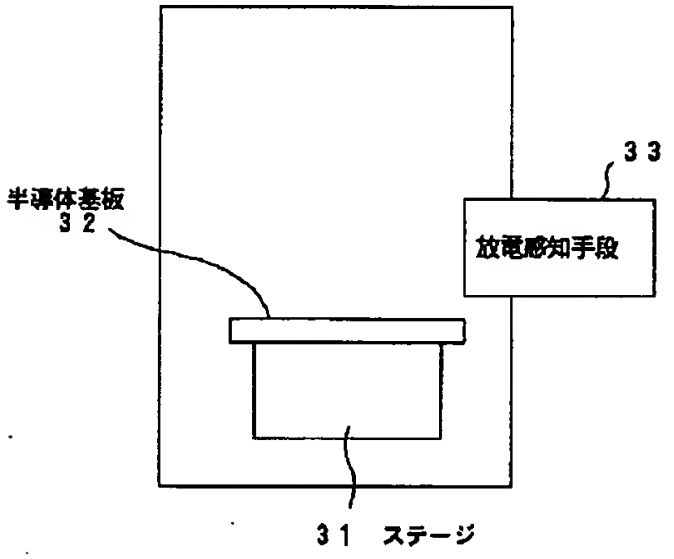
DRAWINGS

[Drawing 6]
放電感知装置の第１の変形例を示す図

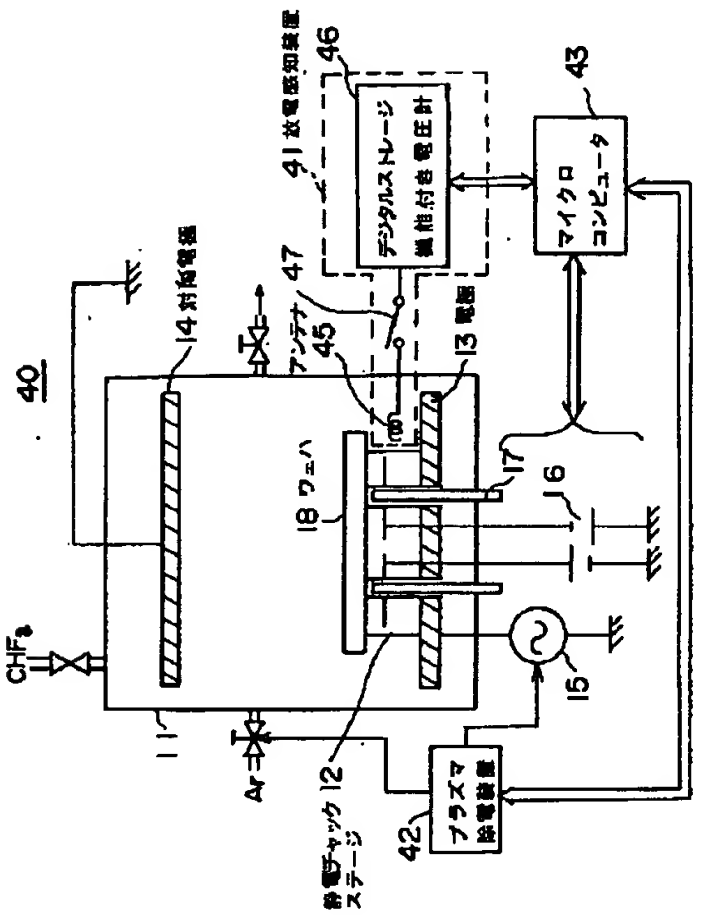


[Drawing 1]
本発明の原理構成図



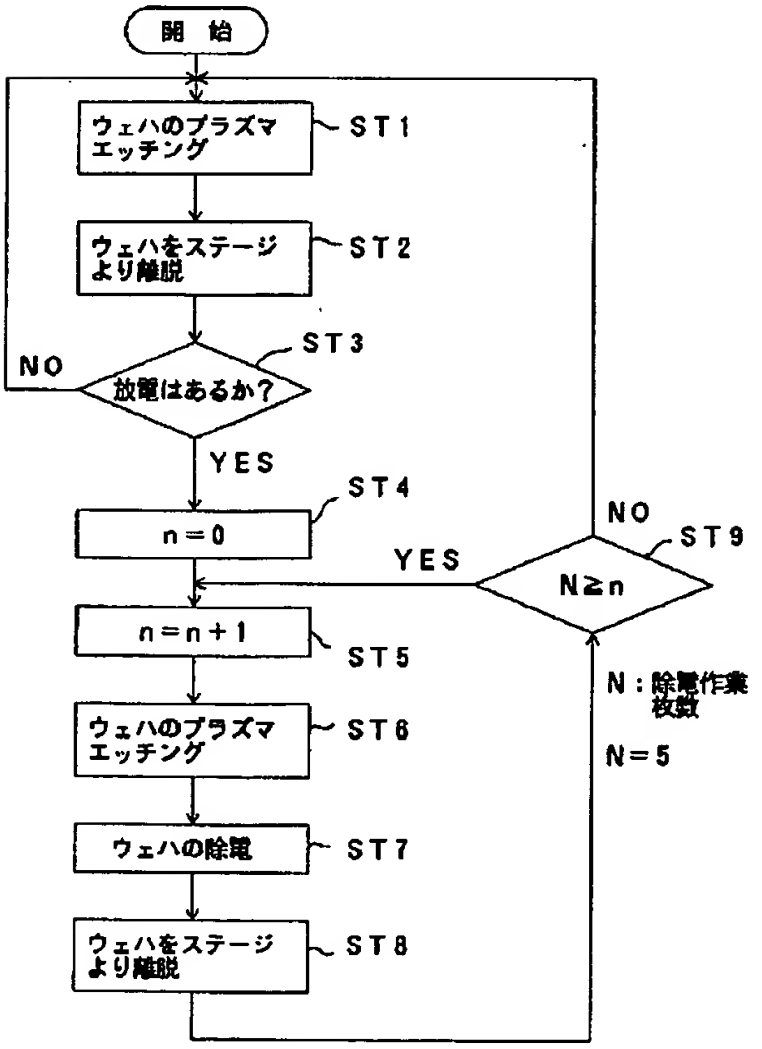
[Drawing 2]

本発明の一実施例によるプラズマエッチング装置を示す図



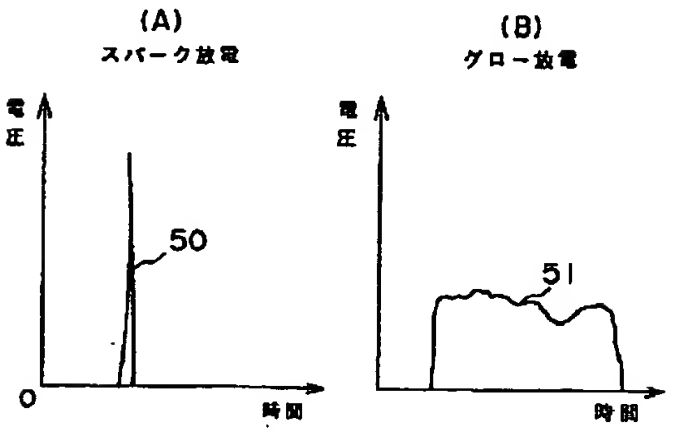
[Drawing 3]

図2の装置の動作のフローチャート



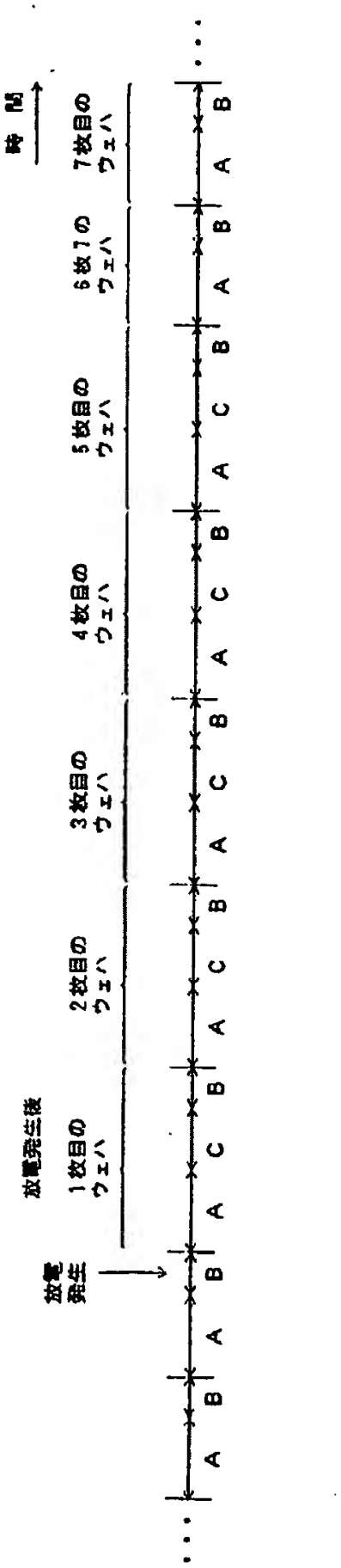
[Drawing 5]

放電の種類と電圧波形との関係を示す図



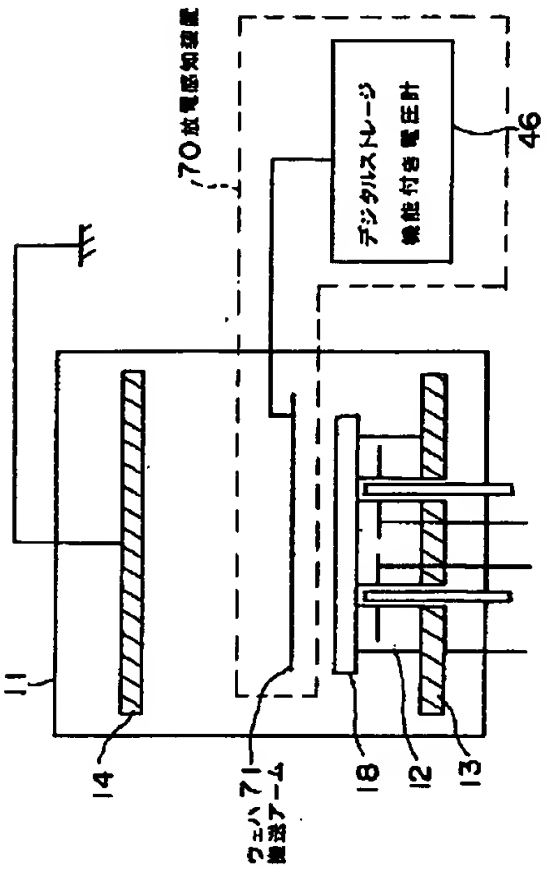
[Drawing 4]

図２の装置の動作を説明する図



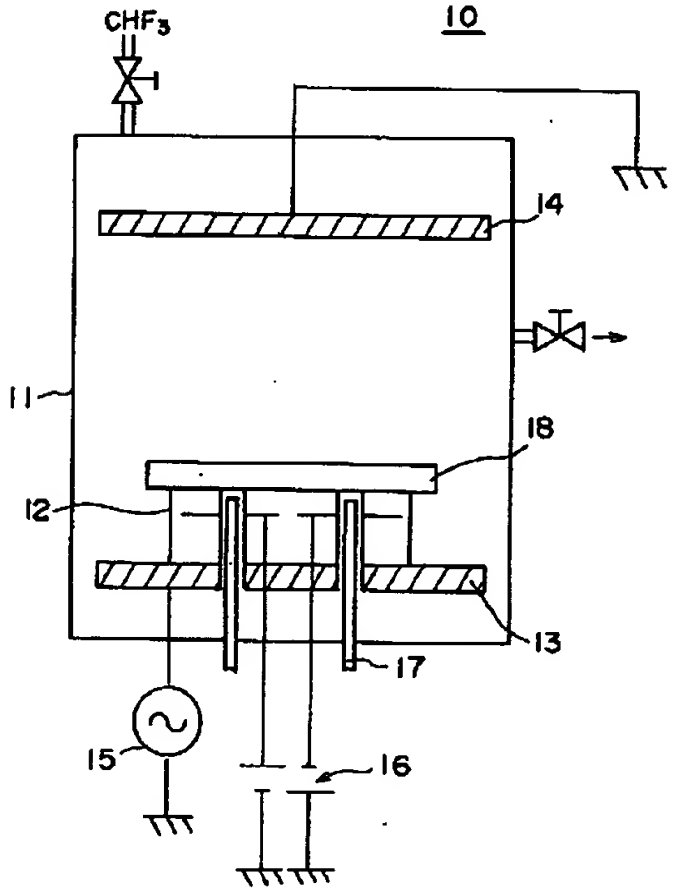
[Drawing 7]

放電感知装置の第２の変形例を示す図



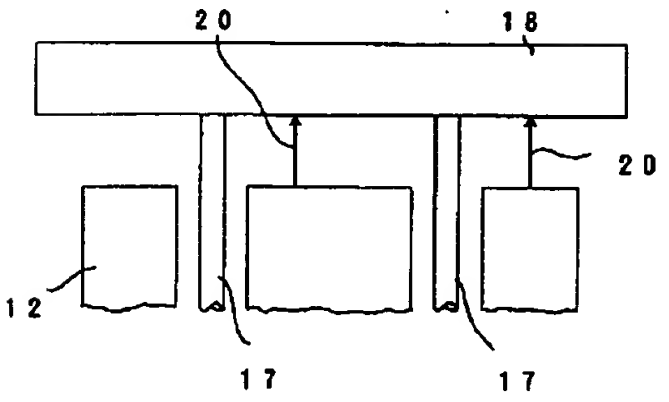
[Drawing 8]

従来のプラズマエッチング装置を示す図



[Drawing 9]

ウェハを静電チャックステージより離脱させるときに発生した放電を示す図



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